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SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a technique for use in the manufacture of a semiconductor device, particularly, to an effective technique that is suitable for the manufacture of a semiconductor device using block molding by transfer molding.

[0002] In the manufacture of a semiconductor device, a method is known in which a plurality of semiconductor chips mounted on a main surface of a substrate are block-molded with one resin enclosure, and then the resin enclosure and the substrate are simultaneously separated into respective semiconductor chips. This manufacturing method is disclosed in Japanese patent Laid-Open No. 107161/1996 (USP 5,729,437) (publicly known document 1) and Japanese patent Laid-Open No. 12578/2000 (USP 6,200,121) (publicly known document 2), for example. More particularly, the publicly known document 1 discloses a method of forming a resin enclosure for block molding by potting, and the publicly known document 2 discloses a method of forming a resin enclosure for block molding by transfer molding.

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## SUMMARY OF THE INVENTION

[0003] The inventors have studied the method for forming a resin enclosure for block molding by transfer molding (hereafter called block transfer molding). Consequently, they have found the following problems.

[0004] Figs. 23A to 26B are diagrams illustrating resin flows when a resin enclosure is formed by block transfer molding in traditional semiconductor device manufacture. In Figs. 23A to 26B, 60 denotes a substrate, 60X denotes a main surface of the substrate 60, 61 denotes a semiconductor chip, 62 denotes a molding die, 62A denotes an upper mold of the molding die 62, 62B denotes a bottom mold of the molding die 62, 63 denotes a cavity, 64 denotes a gate, 65 denotes a runner, 66 denotes an air vent, 67A denotes a resin, 67B denotes a void and S denotes a resin injecting direction.

[0005] Block transfer molding is adopted in the manufacture of a BGA (Ball Grid Array) semiconductor device and a CSP (Chip Size Package or Chip Scale Package) semiconductor device having a package structure with a substrate. In the manufacture of these types of semiconductor devices, the substrate 60, where a plurality of product forming areas 60A are arranged on the main surface 60X in matrix form with a predetermined spacing, is used, as shown in Fig. 23A. Therefore, a plurality of semiconductor chips 61 mounted on the substrate 60 are also arranged in matrix form with a

predetermined spacing.

[0006] In block transfer molding, the molding die 62, having a cavity 63, gates 64, runners 65, a cull (not shown), pots (not shown) and air vents 66, is used as shown in the drawing. The resin 67A is injected inside the cavity 63 from the pots through the culls, the runners 65 and the gates 64.

[0007] Since a substrate 60 having a rectangular plane is generally used, the plane shape of the cavity 63 is also formed into a corresponding rectangular shape. In such case, a plurality of gates 64 are disposed along one of the two long sides of the cavity 63 so that the resin 67A will evenly fill the inside of the entire cavity 63. Thus, the resin 67A is injected inside the cavity 63 from one long side to the other long side of the substrate 60. The resin 67A thus injected inside the cavity 63 flows from one long side to the other long side of the substrate 60 as shown progressively in Figs. 23A to 25B, and eventually fills the inside the cavity 63, as shown in Figs. 26A and 26B.

[0008] Meanwhile, the resin 67A that has been injected inside the cavity 63 flows along a main surface and the side surfaces of each semiconductor chip 61. The resin 67A flowing along the main surface and the side surfaces of a semiconductor chip 61 runs between the semiconductor chips 61. However, the flow of the resin 67A along the main surface of the semiconductor chip 61 is resisted by the semiconductor chip

61. Therefore, it runs slower than the resin 67A flowing along the side surfaces of the semiconductor chip 61 (see Figs. 24A and 24B). For this reason, voids 67B tend to be generated at positions where the resin 67A flowing along the main surface of the semiconductor chip 61 meets the resin 67A flowing along the side surfaces of the semiconductor chip 61 (see Figs. 25A and 25B). The voids 67B gradually become smaller as they are moved by the flow of the resin 67A in the resin injecting process. However, voids 67C remain at positions hiding behind the semiconductor chips 61 with respect to the injecting direction S of the resin 67A (see Figs. 26A and 26B).

[0009] In transfer molding, there is a process for reducing voids that have been caught in the resin by applying a higher injection pressure after resin filling is complete. However, the voids 67C are considerably greater than voids of the type that do not cause the popcorn phenomenon during temperature cycle testing, even though this process is applied. Thus, they become a factor that reduces the yields of semiconductor devices.

[0010] The aforementioned publicly known document 1 (Japanese patent Laid-Open No. 107161/1996) discloses the use of a molding material having a low thixotropic property, and further employs vacuum defoaming as a means of preventing the generation of unfilled portions. However, in transfer molding, application of the aforesaid technique cannot solve

the problem of void generation.

[0011] When transfer molding is adopted, the resin flow is to be controlled by injection from the gates. Therefore, air vents are disposed at positions facing the gates and in areas where the resin is finally filled, and, thereby, air inside the cavity can be removed from the air vents until the resin is filled inside the cavity. However, in transfer molding, when the thixotropic property is reduced to the extent that the resin flow is governed by the thixotropic property, or the resin injecting rate is decreased, it becomes difficult to control the resin flow, and it becomes substantially impossible to set the positions of the air vents that have to be disposed in areas where the resin is finally filled. Accordingly, in transfer molding, it is virtually impossible to control the conditions of the resin in the injecting process and to eliminate generation of voids by adopting a material having a low thixotropic property as the resin.

[0012] Additionally, when a great amount of a filler (80% or more, for example) is added to a molding resin for the purpose of reducing warpage due to the cure shrinkage of the molding resin to facilitate the dicing process, or for the purpose of providing a thermal expansion coefficient of the resin closer to that of a semiconductor chip to reduce the stress applied to the semiconductor chip during heat cycling, the existence of the filler increases the thixotropic property

even though those resins having a low thixotropic property are adopted as a molding material. Therefore, a low thixotropic property is insufficient as a means of solving the void catching problem.

[0013] Furthermore, in potting, a method, such as vacuum defoaming, can be adopted in which air bubbles are removed outside a resin by placing semiconductor devices, that are in a state in which the resin has not been cured, in a low-pressure atmosphere after potting. However, in transfer molding, resin injection and curing are performed inside the cavity, and thus the method for reducing voids by vacuum defoaming cannot be adopted. Consequently, in transfer molding, applying techniques described in the publicly known document 1 cannot prevent the problem of void generation. Therefore, new methods need to be adopted for preventing voids.

[0014] Accordingly, the inventors have turned their attention to the wettability of the resin 67A to the main surface of the substrate 60 to develop a technique to prevent the generation of voids 67C which remain on the main surface of the substrate 60, as shown in Figs. 26A and 26B.

[0015] The object of the present invention is to provide techniques capable of improving the yield of semiconductor devices.

[0016] The aforementioned object, other objects and new features of the invention will be apparent from the following

description and the accompanying drawings.

[0017]        Among the aspects of invention disclosed in the present application, the following is the brief description of a summary of representative features.

[0018]        (1)    A method of manufacturing a semiconductor device comprises forming a resin enclosure for block-molding of a plurality of semiconductor chips by placing a plurality of semiconductor chips inside a cavity of a molding die along with a substrate and then injecting a resin inside the cavity from a first side to a second side along a main surface of the substrate, the plurality of semiconductor chips being mounted on the main surface of the substrate in an arrangement from the first side to the second side of the main surface with a predetermined spacing, the second side facing the first side, wherein the method further comprises removing impurities remaining on the main surface of the substrate before forming the resin enclosure. Removing impurities remaining on the main surface of the substrate is performed by plasma cleaning.

[0019]        (2)    A method of manufacturing a semiconductor device comprises forming a resin enclosure for block-molding of a plurality of semiconductor chips by placing a plurality of semiconductor chips inside a cavity of a molding die along with a substrate and then injecting a resin inside the cavity from a first side to a second side along a main surface of

the substrate, the plurality of semiconductor chips being mounted on the main surface of the substrate in an arrangement from the first side to the second side with a predetermined spacing, the second side facing the first side, wherein the method further comprises the application of surface roughening treatment to the main surface of the substrate before forming the resin enclosure. The surface roughening treatment is performed by plasma cleaning.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The teachings of the invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

[0021] Fig. 1A is a schematic plan view of a semiconductor device representing an embodiment 1 of the invention, and Fig. 1B is a schematic sectional view taken along a line a-a in Fig. 1A;

[0022] Fig. 2 is an enlarged schematic sectional view showing a part of Fig. 1B;

[0023] Fig. 3 is a schematic plan view of a substrate (a substrate for separation) for use in fabricating the semiconductor device of the embodiment 1;

[0024] Fig. 4 is an enlarged schematic plan view showing a part of Fig. 3;

[0025] Fig. 5 is a schematic sectional view taken along a line b-b in Fig. 4;



[0026] Fig. 6 is a schematic plan view illustrating the configuration of an upper mold of a molding die for use in fabricating the semiconductor device of the embodiment 1;

[0027] Fig. 7 is a schematic plan view illustrating the configuration of a bottom mold of the molding die for use in fabricating the semiconductor device of the embodiment 1;

[0028] Fig. 8 is a schematic sectional view illustrating the configuration of the molding die for use in fabricating the semiconductor device of the embodiment 1;

[0029] Figs. 9A and 9B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 1;

[0030] Figs. 10A and 10B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 1;

[0031] Fig. 11 is a schematic sectional view illustrating a step in the fabrication of the semiconductor device of the embodiment 1;

[0032] Fig. 12A is a schematic plan view illustrating the resin molding process used in fabricating the semiconductor device of the embodiment 1, and Fig. 12B is a schematic sectional view thereof;

[0033] Fig. 13A is a schematic plan view illustrating the resin molding process used in fabricating the

semiconductor device of the embodiment 1, and Fig. 13B is a schematic sectional view thereof;

[0034] Fig. 14A is a schematic plan view illustrating the resin molding process used in fabricating the semiconductor device of the embodiment 1, and Fig. 14B is a schematic sectional view thereof;

[0035] Fig. 15A is a schematic plan view illustrating the resin molding process used in fabricating the semiconductor device of the embodiment 1, and Fig. 15B is a schematic sectional view thereof;

[0036] Figs. 16A and 16B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 1;

[0037] Fig. 17 is a schematic sectional view illustrating the configuration of a semiconductor device of an embodiment 2 of the invention;

[0038] Figs. 18A and 18B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 2;

[0039] Figs. 19A and 19B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 2;

[0040] Fig. 20 is a schematic sectional view illustrating the configuration of a semiconductor device of an embodiment 3 of the invention;

[0041] Figs. 21A and 21B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 3;

[0042] Figs. 22A and 22B are schematic sectional views illustrating steps in the fabrication of the semiconductor device of the embodiment 3;

[0043] Fig. 23A is a schematic plan view illustrating the rein molding process used in fabricating a conventional semiconductor device, and Fig. 23B is a schematic sectional view thereof;

[0044] Fig. 24A is a schematic plan view illustrating the rein molding process used in fabricating the conventional semiconductor device, and Fig. 24B is a schematic sectional view thereof;

[0045] Fig. 25A is a schematic plan view illustrating the rein molding process used in fabricating the conventional semiconductor device, and Fig. 25B is a schematic sectional view thereof; and

[0046] Fig. 26A is a schematic plan view illustrating the rein molding process used in fabricating the conventional semiconductor device, and Fig. 26B is a schematic sectional view thereof.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

[0047] Hereafter, various embodiments of the invention will be described in detail with reference to the drawings.

Additionally, in all of the drawings of the embodiments, those elements having the same functions are designated with the same numerals and signs, and a repeated description thereof is omitted.

(Embodiment 1)

[0048] In this embodiment, an example in which the invention is applied to a BGA semiconductor device will be described.

[0049] Figs. 1A and 1B are schematic diagrams illustrating the configuration of the semiconductor device of embodiment 1 of the invention. In Fig. 1A, the semiconductor device is shown with the resin enclosure removed.

[0050] As shown in Figs. 1A, 1B and 2, a semiconductor device 1A is configured to mainly have a substrate (circuit board) 2, a semiconductor chip 10, a plurality of bonding wires 13, a resin enclosure 14 and a plurality of projecting electrodes 15. The semiconductor chip 10 and the plurality of bonding wires 13 are encapsulated with the resin enclosure 14.

[0051] The semiconductor chip 10 is attached and fixed to a main surface 2X of the substrate 2 through a bonding layer 12, and the main surface 2X (chip mounting surface) faces the other main surface (back surface) 2Y of the substrate 2. The semiconductor chip 10 is formed to have a rectangular

shape; more particularly, it is formed to have a square shape in the illustrated embodiment, for example. The semiconductor chip 10 is configured to have a semiconductor substrate made of monocrystal silicon, multilevel interconnection layers having a plurality of insulating layers and wiring layers laminated on the circuit forming side of the semiconductor substrate, and a surface protecting film deposited to cover the multilevel interconnection layers, for example. As the surface protecting film, a polyimide resin is used, for instance.

[0052] The semiconductor chip 10 is provided with a control circuit, for example, as an integrated circuit. The control circuit is mainly configured of transistor devices formed on the circuit forming surface of the semiconductor substrate and wirings formed in the wiring layers.

[0053] A plurality of electrode pads (bonding pads) 11 are formed on a main surface 10X of the semiconductor chip 10 along each of the sides around the semiconductor chip 10, and the main surface 10X (circuit forming surface) faces the other main surface (back surface) of the semiconductor chip 10. Each of the plurality of electrode pads 11 is formed on the topmost wiring layer, among the multilevel interconnection layers of the semiconductor chip 10, which is electrically connected to the transistor devices constituting the control circuit. Each of the plurality of electrode pads 11 is formed

of a metal film, such as an aluminium (Al) film or aluminium alloy film.

[0054] The substrate 2 is not shown in detail, but it has a multilevel interconnection structure where each of the insulating layers and conductive layers is sequentially laminated. Each of the insulating layers is formed of a glass-epoxy substrate where glass fibers are impregnated with an epoxy resin, and each of wiring layers is formed of a metal film made of copper (Cu), for example. The substrate 2 is formed to have a rectangular shape; more particularly, it is formed to have a square shape in the illustrated embodiment, for example.

[0055] The main surface 2X of the substrate 2 has disposed thereon plurality of connecting parts (lands) 3 made of a part of wirings formed in the topmost conductive layer thereof. Additionally, a resin film 4 for protecting the wirings formed in the topmost conductive layer thereof is deposited on the main surface 2X of the substrate 2. The resin film 4 is formed with apertures for exposing the surfaces of the connecting parts 3.

[0056] The back surface 2Y of the substrate 2 has disposed thereon a plurality of electrode pads (lands) 5 made of a part of the wirings formed in the undermost conductive layer thereof. Furthermore, the back surface 2Y of the substrate 2 has deposited thereon a resin film 6 for protecting the

wirings formed in the undermost conductive layer thereof. The resin film 6 is formed with apertures for exposing the surfaces of the electrode pads 5. The resin films 4 and 6 are formed of an epoxy resin or polyimide resin, for example.

[0057] Each of the plurality of bump electrodes 15 is fixed to the plurality of electrode pads 5 disposed on the back surface 2Y of the substrate 2, to which they are electrically and mechanically connected. The projecting bump electrodes 15 are formed of a ball-like bump made of a solder material having Pb-Sn composition, for example.

[0058] The resin enclosure 14 is formed to have a rectangular shape; more particularly, it is formed to have a square shape in the illustrated embodiment, for example. The resin enclosure 14 is formed of an epoxy thermosetting insulating resin having in addition a phenol curing agent, a silicon rubber and many fillers (silica, for example) for the purpose of providing a low stress.

[0059] Each of the plurality of electrode pads 11 disposed on the main surface 10X of the semiconductor chip 10 is electrically connected to the plurality of connecting parts 3 disposed on the main surface 2X of the substrate 2 through the bonding wires 13. As the bonding wires 13, gold (Au) wires are used, for example. As a method of connecting the bonding wires 13, ball bonding (nail head bonding) that combines thermo-compression bonding with ultrasonic vibration is used.

[0060]        The resin enclosure 14 and the substrate 2 have almost the same outer shapes and sizes, and the side surfaces of the resin enclosure 14 and the substrate 2 are substantially flush. In fabricating the semiconductor device 1A of the embodiment, a fabricating method is adopted in which a plurality of semiconductor chips 10 mounted on the main surface of the substrate with a predetermined spacing are block-molded using a resin enclosure, and then the resin enclosure and the substrate are simultaneously separated into respective semiconductor chips 10 (each of the product forming areas). The method will be more specifically described later.

[0061]        Fig. 3 is a schematic plan view illustrating a substrate for use in fabricating the semiconductor device 1A of the embodiment. Fig. 4 is a schematic plan view of a part of Fig. 3. Fig. 5 is a schematic sectional view taken along a line b-b in Fig. 4.

[0062]        As shown in Figs. 3 to 5, the substrate (circuit board) 20 is formed to have a rectangular shape; more particularly, it is formed to have a square shape in the illustrated embodiment, for example. On a main surface (chip mounting surface) 20X of the substrate 20, a plurality of product forming areas 22 are arranged in a matrix form with a predetermined spacing. Each of the product forming areas 22 is disposed with a chip mounting area 23, and a plurality of connecting parts 3 are arranged therearound. Each of the



product forming areas 22 is disposed in a molding area 21 where a resin enclosure is formed. Each of the product forming areas 22 is configured to have the same configuration as the substrate 2. That is, a resin film 4 is deposited over the entire main surface 20X of the substrate 20, and a resin film 6 is deposited over the entire other main surface (back surface) facing the main surface 20X. Additionally, the product forming areas 22 are spaced from each other through a separation area for separating the substrate 20.

[0063] Fig. 6 is a schematic plan view illustrating the configuration of an upper mold of a molding die for use in fabricating the semiconductor device 1A of the embodiment. Fig. 7 is a schematic plan view illustrating the configuration of a lower or bottom mold of the molding die. Fig. 8 is a schematic sectional view illustrating the configuration of the molding die.

[0064] As shown in Figs. 6 to 8, a molding die 30 has a cavity 31, a plurality of gates 32, a plurality of subrunners 33, a plurality of main runners 34, a plurality of culls 35, a joining runner 36, a plurality of air vents 37, a plurality of pots 38 and a substrate mounting area 39. Each of the component parts 31 to 37 is disposed in an upper mold 30A and each of the component parts 38 and 39 is disposed in the bottom mold 30B. The cavity 37 and the substrate mounting area 39 are formed to have a plane shape corresponding to

the plane shape of the substrate 20; that is, they are formed to have a rectangular shape in the illustrated embodiment, for example. The cavity 31 is recessed from the mating face of the upper mold 30A in the depth direction. The substrate mounting area 39 is recessed from the mating face of the bottom mold 30B in the depth direction.

[0065] In the molding die 30, a resin is injected inside the cavity 31 from the pots 38 through the culls 35, the main runners 34, the subrunners 33 and the gates 32. The plurality of gates 32 are arranged along one of the two long sides of the cavity 31 corresponding each other so as to evenly fill the inside of the entire cavity 31 with resin. Thus, the resin is injected inside the cavity 31 from one long side to the other long side of the cavity 31. The plurality of air vents 37 are arranged along three sides, except for the long side of the cavity 31 where the gates 32 are disposed.

[0066] Next, the fabrication of the semiconductor device 1A of the embodiment will be described with reference to Figs. 9A to 16B. Figs. 9A, 9B, 10A, 10B, 11, 16A and 16B are schematic sectional views illustrating the fabrication of the semiconductor device. Figs. 12A to 15B are diagrams illustrating the resin flow when a resin enclosure is formed by block transfer molding.

[0067] First, the substrate 20 shown in Fig. 3 is prepared. Then, a bonding layer 12 made of an epoxy thermosetting resin,

for example, is deposited on the chip mounting area in each of the product forming areas on the main surface 20X of the substrate 20. The semiconductor chip 10 is mounted on each of the chip mounting areas through the bonding layer 12. Heat treatment is applied to cure the bonding layer 12. The semiconductor chip 10 is attached and fixed in each of the chip mounting areas, as shown in Fig. 9A. In this process, the substrate 20 is heated at a temperature of about 150°C, for example, and therefore a natural oxide film is formed on the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 20. Additionally, impurities, such as fats, oils and organic solvents contained in the resin film 4, are outgassed to contaminate the main surface 20X and the surfaces of the connecting parts 3 of the substrate 20 and the surfaces of electrode pads 11.

[0068] Subsequently, as shown in Fig. 9B, cleaning treatment is applied to the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 20 to remove impurities, such as the natural oxide film, fats, oils and organic solvents, remaining on these surfaces. The cleaning treatment is performed by plasma cleaning using an oxygen or argon gas, for example.

[0069] Then, as shown in Fig. 10A, the electrode pads

11 of the semiconductor chip 10 are electrically connected to the connecting parts 3 of the substrate 20 using the bonding wires 13. In this process, since impurities, such as the natural oxide film, fats, oils and organic solvents, remaining on the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 20, have been removed in the previous cleaning process, the connection reliability in the wire bonding process is enhanced. Furthermore, in this process, the substrate 20 is heated at a temperature of about 125°C, for example. Thus, impurities, such as fats, oils and organic solvents contained in the resin film 4, are outgassed so as to contaminate the main surface 20X of the substrate 20. Moreover, in this process, a plurality of semiconductor chips 10 are mounted on the main surface 20X of the substrate 20.

[0070] Subsequently, as shown in Fig. 10B, cleaning treatment is applied to the main surface 20X of the substrate 20 to remove impurities, such as fats, oils and organic solvents remaining on the main surface 20X of the substrate 20. This cleaning treatment is performed by plasma cleaning using an oxygen or argon gas. Plasma cleaning can remove impurities, such as fats and oils, and can roughen the surface of the main surface 20X of the substrate 20.

[0071] Then, as shown in Fig. 11, the substrate 20 is positioned between the upper mold 30A and the lower or bottom

mold 30B of the molding die 30, and the plurality of semiconductor chips 10 mounted on the main surface 20X of the substrate 20 are placed inside the cavity 31 of the molding die 30 along with the substrate 20. At this time, the substrate 20 is mounted on the substrate mounting area 39 disposed in the bottom mold 30B.

[0072] Subsequently, an epoxy thermosetting resin, for example, is injected inside the cavity 31 from the pods 38 through the culls 35, the main runners 34, the subrunners 33 and the gates 32 to form a resin enclosure 24 for block-molding the plurality of semiconductor chips 10 mounted on the main surface 20X of the substrate 20.

[0073] In this process, as shown in Fig. 12A, the plurality of gates 32 are arranged along one of the two long sides of the cavity 31 facing each other so as to evenly fill the inside of the entire cavity 31 with the resin 24A, and, therefore, the resin 24A is injected inside the cavity 31 from one long side to the other long side of the substrate 20. At this time, the semiconductor chips 10 are arranged so that two sides facing each other are almost orthogonal to the injecting direction S of the resin 24A.

[0074] The resin 24A injected inside the cavity 31 flows from one long side to the other long side of the substrate 20 as shown in Figs. 12A to 14B, and the inside of the cavity 31 is filled, as shown in Figs. 15A and 15B.

[0075]        The resin 24A injected inside the cavity 31 flows along the main surface 10X and the side surfaces of the semiconductor chip 10. The resin 24A flowing along the main surface 10X and the side surfaces of the semiconductor chip 10 runs into the areas between the semiconductor chips 10. However, the resin 24A flowing along the main surface 10X of the semiconductor chip 10 runs slower than the resin 24A flowing along the side surfaces of the semiconductor chip 10. Therefore, voids 24B are generated at positions where the resin 24A flowing along the main surface 10X of the semiconductor chip 10 meets the resin 24A flowing along the side surfaces of the semiconductor chip 10 (see Figs. 14A and 14B). On the other hand, since impurities, such as fats and oils, remaining on the main surface 20X of the substrate 20, have been removed in the aforesaid cleaning process, and since the main surface 20X of the substrate 20 has been roughened, the wettability of the resin 24A is enhanced with respect to the main surface 20X of the substrate 20. For this reason, the resin 24A flowing along the side surfaces of the semiconductor chip 10 is allowed to easily enter the positions behind the semiconductor chips 10 with respect to the injecting direction S of the resin 24A. Accordingly, the voids 24B generated at the positions where the resin 24A flowing along the main surface 10X of the semiconductor chip 10 meets the resin 24A flowing along the side surfaces of the semiconductor

chip 10 (see Figs. 14A and 14B) are dislodged from the main surface 20X of the substrate 20. The voids 24B thus dislodged from the main surface 20X of the substrate 20 are able to easily move in response to the flow of the resin 24A in the resin injecting process. Therefore, the voids 24B do not remain at positions hiding behind the semiconductor chips 10, as shown in Fig. 15A and 15B. The voids 24E dislodged from the main surface 20X of the substrate 20 become smaller and smaller due to the flow of the resin 24A as they move. They become smaller to the extent of not causing the popcorn phenomenon during temperature cycle testing.

[0076] That is, cleaning treatment is applied to the main surface 20X of the substrate 20 to remove impurities, such as fats and oils, remaining on the main surface 20X of the substrate 20 before forming the resin enclosure 24. Thereby, the wettability of the resin 24A to the main surface 20X of the substrate 20 is enhanced and the resin 24A flowing along the side surfaces of the semiconductor chip 10 is allowed to easily enter the positions hiding behind the semiconductor chips 10 with respect to the injecting direction S of the resin 24A. Thus, the voids 24B generated at the positions where the resin 24A flowing along the main surface 10X of the semiconductor chip 10 meets the resin 24A flowing along the side surfaces of the semiconductor chip 10 are dislodged from the main surface 20X of the substrate 20.

[0077]        Additionally, cleaning treatment is performed by plasma cleaning, and, thereby, the main surface 20X of the substrate 20 is roughened, in addition to the removal of impurities, such as fats and oils, remaining on the main surface 20X of the substrate 20. Therefore, the wettability of the resin 24A with respect to the main surface 20X of the substrate 20 is further enhanced. The wettability of the resin 24A is enhanced by removing impurities, such as fats and oils, remaining on the surface where the resin flows and by roughening the surface where the resin flows. However, naturally, the enhancement of the wettability of the resin by surface roughening is limited.

[0078]        Then, as shown in Fig. 16A, projecting electrodes 15 are formed on the surfaces of electrode pads 5 disposed on the back surface of the substrate 20 by ball feeding, for example. Then, the substrate 20 is attached and fixed to a dicing sheet 25 so that the resin enclosure 24 being block-molded faces the dicing sheet 25. After that, as shown in Fig. 16B, the resin enclosure 24 and the substrate 20 are simultaneously separated into respective semiconductor chips 10 (each of the product forming areas). The semiconductor device 1A shown in Figs. 1A to 3 is almost complete in this process.

[0079]        In this manner, according to the embodiment, the following effects can be obtained.



[0080] In the method for manufacturing the semiconductor device 1A, the method comprises forming the resin enclosure 24 for block-molding the plurality of semiconductor chips 10 by placing the plurality of semiconductor chips 10 inside the cavity 31 of the molding die 30 along with the substrate 20 and then injecting the resin 24A inside the cavity 31 from one long side to the other long side of the main surface 20X of the substrate 20, the plurality of semiconductor chips 10 being mounted on the main surface 20X of the substrate 20 from one long side to the other long side of the main surface 20X with a predetermined spacing, the other long side facing to one long side, wherein the method further comprises removing impurities remaining on the main surface 20X of the substrate 20 by plasma cleaning before forming the resin enclosure 24.

[0081] Accordingly, impurities, such as fats, oils and organic solvents, remaining on the main surface 20X of the substrate 20 are removed, and a material having a high wettability to the resin 24A is more fully exposed on the main surface 20X of the substrate 20, or the main surface 20X of the substrate 20 is formed to have fine bumps and dips. Thereby, the wettability of the resin 24A to the main surface 20X of the substrate 20 is enhanced, and the flow accompanying the injection of the resin 24A can accelerate the removal of the voids in the resin 24A. Consequently, an improvement

of the yield of the semiconductor devices 1A can be achieved.

[0082] An example in which a substrate 20 having a resin film 4 on a main surface 20X thereof was described as an embodiment. However, resin substrates allow impurities such as fats, oils and organic solvents contained in the resin substrates, to be outgassed by heat treatment in the fabricating process, even though the main surface 20X does not have a resin film 4.

[0083] Furthermore, although an example has been described in which a glass-epoxy substrate is used as the substrate 20, the invention is also effective when a substrate made of BT resin is used.

[0084] Besides, when resin tape is used as the substrate 20, warpage is intensified due to the cure shrinkage of the resin enclosure, and thus the amount of filler added has to be increased. In such a case, voids tend to be generated because the flowability of the resin is decreased.

(Embodiment 2)

[0085] Fig. 17 is a schematic sectional view of a semiconductor device representing an embodiment 2 of the invention.

[0086] As shown in Fig. 17, a semiconductor device 1B of the embodiment 2 is basically configured to have the same configuration as the aforesaid embodiment 1, but differs in the following way. That is, a semiconductor chip 10 is

attached and fixed to a main surface 2X of a substrate 2 through a bonding layer 12, and a semiconductor chip 40 is attached and fixed to a main surface 10X of the semiconductor chip 10 through a bonding layer 42. The semiconductor chip 40 is formed to have a plane size smaller than that of the semiconductor chip 10. Electrode pads 41, which are arranged on a main surface of the semiconductor chip 40, are electrically connected to connecting parts 3 formed on a main surface 2X of the substrate 2 through bonding wires 43. The semiconductor chips 10 and 40 are encapsulated by a resin enclosure 14.

[0087] Hereafter, the method of manufacture of the semiconductor device 1B will be described with reference to Figs. 18A to 19B. Figs. 18A to 19B are schematic sectional views illustrating steps in the manufacture of the semiconductor device.

[0088] First, a substrate 20 is prepared. Then, the bonding layer 12, made of an epoxy thermosetting resin, for example, is deposited on a chip mounting area in each of the product forming areas on a main surface 20X of the substrate 20. A semiconductor chip 10 is mounted on the chip mounting area through the bonding layer 12. Heat treatment is applied to cure the bonding layer 12, and the semiconductor chip 10 is attached and fixed in the chip mounting area. In this process, the substrate 20 is heated at a temperature of about 180°C, for example, and thus a natural oxide layer is deposited

on the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 20. Additionally, impurities, such as fats, oils and organic solvents, contained in a resin film 4 are outgassed to contaminate the main surface of the substrate 20, and the surfaces of the connecting parts 3 and the electrode pads 11.

[0089] Then, the main surface 10X of each of the semiconductor chips 10 is formed with a bonding layer 42 made of an epoxy thermosetting resin. The semiconductor chip 40 is mounted on the main surface 10X of the semiconductor chip 10 through the bonding layer 42. Heat treatment is applied to cure the bonding layer 42. The semiconductor chip 40 is attached and fixed to the semiconductor chip 10, as shown in Fig. 18A. In this process, the substrate 20 is heated at a temperature of about 180°C, for example, and thus a natural oxide layer is deposited on the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 20. Furthermore, impurities, such as fats and oils, contained in the resin film 4 are outgassed so as to contaminate the main surface of the substrate 20 and the surfaces of the connecting parts 3 and the electrode pads 11.

[0090] Subsequently, as shown in Fig. 18B, the impurities remaining on the surfaces of the electrode pads 11 and 41

of the semiconductor chips 10 and 40 and the surfaces of the connecting parts 3 of the substrate 20 are removed by plasma cleaning using an oxygen or argon gas.

[0091] Then, as shown in Fig. 19A, the electrode pads 11 of the semiconductor chip 10 are electrically connected to the connecting parts 3 of the substrate 20 using bonding wires 13, and the electrode pads 41 of the semiconductor chip 40 are electrically connected to the connecting parts 3 of the substrate 20 using the bonding wires 43. In this process, the substrate 20 is heated at a temperature of about 125°C, for example, and thus impurities, such as fats and oils, contained in the resin film 4 are outgassed so as to contaminate the main surface of the substrate 20.

[0092] Subsequently, as shown in Fig. 19B, the impurities remaining on the main surface 20X of the substrate 20 are removed by plasma cleaning using an oxygen or argon gas. In this process, plasma cleaning can roughen the main surface 20X of the substrate 20, and, therefore, the removal of impurities and roughening of the main surface 20X of the substrate 20 can be performed.

[0093] Then, similar to the aforementioned embodiment 1, the substrate 20 is positioned between an upper mold 30A and a lower or bottom mold 30B of a molding die 30. The plurality of semiconductor chips 10 mounted on the main surface 20X of the substrate 20 and each of the plurality of semiconductor

chips 40 layered on the respective semiconductor chips 10 are placed inside a cavity 31 of the molding die 30 along with the substrate 20. A resin is then injected inside the cavity 31 from pots 38 through culls 35, main runners 34, subrunners 33 and gates 32. A resin enclosure is formed for block-molding the plurality of semiconductor chips 10 and 40 mounted on the main surface 20X of the substrate 20.

[0094] After that, the same process as the aforesaid embodiment 1 is carried out, and, thereby, the semiconductor device 1B shown in Fig. 17 can be manufactured.

[0095] In manufacturing the semiconductor device 1B of the embodiment 2, two semiconductor chips 10 and 40 are laminated on the main surface 20X of the substrate 20. Thus, voids tend to be generated at the positions hiding behind the semiconductor chips 10 and 40 with respect to the injecting direction S of the resin 24A. However, since cleaning treatment is applied to the main surface 20X of the substrate 20 before the resin enclosure is formed, the same effects as the aforementioned embodiment 1 can be obtained.

(Embodiment 3)

[0096] Fig. 20 is a schematic sectional view of a semiconductor device according to an embodiment 3 of the invention.

[0097] As shown in Fig. 20, the semiconductor device 1C of the embodiment 3 is basically configured to have the same

configuration as the embodiment 2, but varies in the following way. That is, a semiconductor chip 50 is mounted on a main surface 2X of a substrate 2 through projecting electrodes 53, and a semiconductor chip 10 is attached and fixed to the other main surface (back surface), facing one main surface of the semiconductor chip 50, through a bonding layer 12. Electrode pads 51 arranged on the main surface of the semiconductor chip 50 are electrically connected to electrode pads 3A arranged on the main surface 2X of the substrate 2 through the projecting electrodes 53. An epoxy thermosetting resin 52, for example, is injected into the space between the semiconductor chip 50 and the substrate 2. Electrode pads 11 of the semiconductor chip 10 are electrically connected to connecting parts 3 of the substrate 2 through bonding wires 13. The semiconductor chips 50 and 10 are encapsulated by a resin enclosure 14.

[0098] Hereafter, the method of manufacture of the semiconductor device 1C will be described with reference to Figs. 21A, 21B and 22A, 22B. Figs. 21A to 22B are schematic sectional views illustrating steps in the manufacture of the semiconductor device.

[0099] First, the substrate 2 is prepared, and then the projecting electrodes 53 are molten in a state in which the projecting electrodes 53 are disposed between the electrode pads 3A arranged in a chip mounting area of each of the product

forming areas on the main surface 2X of the substrate 2 and the electrode pads 51 arranged on the main surface of the semiconductor chip 50, and the semiconductor chip 50 is mounted on each of the product forming areas on the main surface of the substrate 2. In this process, the substrate 2 is heated at a temperature of about 205°C, for example, and thus a natural oxide layer is deposited on the surfaces of the connecting parts 3 of the substrate 2. Additionally, impurities, such as fats, oils and organic solvents, contained in a resin film 4 are outgassed so as to contaminate the main surface and the surfaces of the connecting parts 3 of the substrate 2.

[0100] Then, the epoxy thermosetting resin 52, for example, is injected into the space between the semiconductor chip 50 and the substrate 2, and, subsequently, heat treatment is applied to cure the thermosetting resin 52. In this process, the substrate 2 is heated at a temperature of about 150°C, for example, and thus a natural oxide layer is deposited on the surfaces of the connecting parts 3 of the substrate 2. Furthermore, impurities, such as fats, oils and organic solvents, contained in the resin film 4 are outgassed so as to contaminate the main surface and the surfaces of the connecting parts 3 of the substrate 2.

[0101] Then, the bonding layer 12, made of an epoxy thermosetting resin, for example, is deposited on the back surface of each of the semiconductor chips 50. The



semiconductor chip 10 is mounted on the back surface of the semiconductor chips 50 through the bonding layer 12. Heat treatment is applied to cure the bonding layer 12, and the semiconductor chip 10 is attached and fixed to the semiconductor chip 50, as shown in Fig. 21(A). In this process, the substrate 2 is heated at a temperature of about 180°C, for example, and thus a natural oxide layer is deposited on the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 2. Moreover, impurities, such as fats and oils, contained in the resin film 4 are outgassed so as to contaminate the main surface of the substrate 2 and the surfaces of the electrode pads 11 and the connecting parts 3.

[0102] Subsequently, as shown in Fig. 21(B), the impurities remaining on the surfaces of the electrode pads 11 of the semiconductor chip 10 and the surfaces of the connecting parts 3 of the substrate 2 are removed by plasma cleaning using an oxygen or argon gas.

[0103] Then, as shown in Fig. 22(A), the electrode pads 11 of the semiconductor chip 10 are electrically connected to the connecting parts 3 of the substrate 2 by bonding wires 13. In this process, the substrate 2 is heated at a temperature of about 125°C, for example, and thus impurities, such as fats and oils, contained in the resin film 4 are outgassed so as to contaminate the main surface of the substrate 2.

[0104] Subsequently, as shown in Fig. 22(B), the impurities remaining on the main surface 2X of the substrate 2 are removed by plasma cleaning using an oxygen or argon gas. In this process, plasma cleaning can roughen the main surface 2X of the substrate 2, and, therefore, the removal of impurities and roughening the main surface 2X of the substrate 2 can be performed.

[0105] Then, as similar to the aforementioned embodiments 1 and 2, the substrate 2 is positioned between an upper mold 30A and a lower or bottom mold 30B of a molding die 30. The plurality of semiconductor chips 50 mounted on the main surface 2X of the substrate 2 and each of the plurality of semiconductor chips 10 layered on the respective semiconductor chips 50 are placed inside a cavity 31 of the molding die 30 along with the substrate 2. A resin is then injected inside the cavity 31 from pots 38 through culls 35, main runners 34, subrunners 33 and gates 32. A resin enclosure is formed for block-molding the plurality of semiconductor chips 50 and 10 mounted on the main surface 2X of the substrate 2.

[0106] After that, the same process as the aforesaid embodiment 1 is applied, and, thereby, the semiconductor device 1C shown in Fig. 20 can be manufactured.

[0107] In manufacturing the semiconductor device 1C of the embodiment 3, two semiconductor chips 50 and 10 are

laminated on the main surface 2X of the substrate 2. Thus, voids tend to be generated at the positions hiding behind the semiconductor chips 50 and 10 with respect to the injecting direction S of the resin 24A. However, since cleaning treatment is applied to the main surface 2X of the substrate 2 by plasma cleaning before the resin enclosure is formed, the same effects as the aforementioned embodiment 1 can be obtained.

[0108] As described above, the invention made by the inventors has been specifically described with reference to embodiments thereof. However, it is needless to say that the invention is not limited to the embodiments, which can be modified variously within the scope of the invention, not deviating from the teachings thereof. For example, the invention can be applied to a technique for manufacturing a semiconductor device having a CSP structure.

[0109] Additionally, the invention can be applied to a technique for manufacturing a semiconductor device having an MCM structure where a plurality of semiconductor chips are mounted on a substrate.

[0110] In brief, the effect obtained by the representative aspects of the invention disclosed in the present application is as follows. According to the invention, an improvement of the yield of semiconductor devices can be achieved.